REMARKS

After the foregoing amendment, claims 3-25, as amended, are pending in the application. Claims 3, 8, 12, 16, 17, 22 and 25 have been amended to more particularly point out and distinctly claim the subject matter which Applicant regards as the invention. Claims 1-2 have been canceled. Applicant submits that no new matter has been added to the application by the Amendment.

The Specification

The Examiner objected to various informalities in the specification. Applicant has amended the specification to correct the informalities identified by the Examiner and has also corrected other typographical errors in the specification that have come to his attention, as noted on page 2 of the Amendment. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the objection to the specification.

Claim Objections

The Examiner objected to claims 1-3, 5-7, 9-12 15-17 and 19-25 for a variety of informalities. Applicant traverses the objections.

a. In respect to claims 3, 5-7, 9-12, 15-17 and 19-24, Applicant wishes to note the following:

Independent claims 3, 12 and 17 clearly define: (1) 2n as the number of input and output ports, thereby defining $n = \log_2$ of the number of switches; (2) $b_1, b_2, \ldots b_n$ as a set of binary addresses of the input and output ports; (3) $\gamma(k)$ as a mapping of the set of numbers 1, 2...k to the set 1, 2...n; and (4) k as the number of stages in the network. Consequently, those terms are also defined for dependent claims 5-7, 9-11, 15-17 and 19-24. Further, Applicant submits that the invention is not limited as to the number of input and output ports "n" or the number of stages "k" in the network. Consequently, no upper bound for n or k is applicable to establishing the metes and bounds of the invention.

b. In respect to claims 9, 11, 16 and 22-24, Applicant wishes to note the following:

Claims 9, 16 and 22 clearly define r by stating that 2^r are the number of priority classes. The term k is defined in claim 3 from which claims 9 and 11 depend, claim 12 from which claim 16 depends and claim 17, from which claims 22-24 depends. Further, Applicant submits that his invention is not limited as to the number of input and output ports "n" or the number of priorities "r". Consequently, no upper bound for either r or k is applicable to establishing the metes and bounds of the invention.

Claim 25 has been amended to bound p and q to within the limits of the number of stages.

Claims 8, 16 and 22 have been amended to correct the antecedent basis of the term "tiebreaker".

In view of the fact that Applicant has addressed all of Examiner's objections, Applicant respectfully requests reconsideration and withdrawal of the objections to claims 3, 5-7, 9-12 15-17 and 19-25.

Double Patenting Rejection

The Examiner provisionally rejected claims 1-7, 12-15 and 17-21 under the judicially created doctrine of obvious type double patenting over claims 1-16 of U.S. Patent Application No. 09/882,005. The Examiner stated that a timely filed terminal disclaimer in compliance with 37 C.F.R. 1.321 may be used to overcome the actual or provisional rejection providing the conflicting patent is shown to be commonly owned.

A Terminal Disclaimer and Statement of Common Ownership signed by Applicants' registered attorney of record is attached herewith. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the double patenting rejection of claims 1-7,12-15 and 17-21.

Rejection - 35 U.S.C. § 103

The Examiner rejected claims 1-8, 12-21 and 25 under 35 U.S.C. § 103 as being unpatentable over U.S. Patent No. 6,335,930 (Lee) in view of U.S. Patent No. 5,940,389 (Yang et al.). Applicant respectfully traverses the rejection.

Claim3

Claim 3 recites:

A method for self-routing a plurality of packets through a $2^n x 2^n$ switch, the switch having 2^n external input ports and 2^n external output ports labeled with 2^n distinct binary output addresses in the form of $b_1 b_2 ... b_n$, and composed of a plurality of switching cells interconnected into a k-stage bit-permuting network which is characterized by the guide $\gamma(1), \gamma(2), \ldots, \gamma(k)$ where γ is a mapping from the set {1, 2,..., k} to the set {1, 2,..., n}, each of the packets destined for a rectangular set of output addresses represented by a quaternary sequence $Q_1, Q_2, \ldots, Q_n$, where each Q_j is a quaternary symbol in any one of the three values: '0-bound', '1-bound', and 'bicast', wherein each of the switching cells is a sorting cell associated with the partial order "'0-bound' $\prec$ 'bicast' $\prec$ '1-bound'", the method comprising:

generating a routing tag $Q_{\gamma(1)} Q_{\gamma(2)} \ldots Q_{\gamma(k)}$ for each of the packets based on the guide of the bit-permuting network and the destination output addresses of the packet, and

routing each of the packets through the network by using $Q_{\gamma(j)}$ in the routing tag of the packet in the j-th stage cell, $1 \leq j \leq k$, to select an output or both outputs from the j-th stage cell to emit the packet.

Amended independent claim 3 recites a method for self-routing a packet to a given destination address through a bit-permitting network having 2^n input ports and 2^n output ports. As defined at page 53, lines 11-14 of the application, in order to be considered a bit-permuting network: (1) the switching elements must be 2x2 switches; (2) every stage of the network must consist of 2^{n-1} 2x2 switches, and (3) every exchange in the network must be bit-permuting.

The switching elements disclosed by Lee each comprise X bypassing input ports, M-X input routing ports, X bypassing output ports and M-X output routing ports where X is an integer

greater than 0. (See col. 6, lines 4-7). Since the number of bypassing ports for each element, X, must be one or more, the switching elements taught by Lee are at least 3x3 (see col. 8, lines 25-28). Also, Figs. 6 and 7 clearly show three inputs and three outputs from each switching element internal to the network. Consequently, the switching elements disclosed by Lee are not 2x2 switching elements, and therefore, the network disclosed by Lee is not a bit permuting network as expressly defined in the application.

Amended claim 3 also recites routing a packet through the network based on a routing tag where the routing tag is based on a guide of the network.

As described at page 81, line 14 of the application, a guide is the sequence:

$(\sigma_1\sigma_2 \ldots\sigma_{k-1})(n), (\sigma_2 \ldots.\sigma_{k-1})(n), \ldots., (\sigma_{k-2}\sigma_{k-1})(n), \sigma_{k-1}(n), n,$

where, 2^n is the number of input/output ports of the network, k is the number of stages in the network and σ_k is the permutation between the k-1 stage and k stage of the network. Simply stated, as can be appreciated by referring to the description at pages 88-89, the guide characterizes the state of each cell, (bar or cross) in each stage of the network while the parameter σ describes the interconnections between each stage. As further described starting at page 174, and Figs. 66 A, B C and D, the routing tag, and thereby the route taken by a packet through the network, is determined from the input address of the network at which the packet is received, the output address to which the packet is to be delivered and the guide.

Further, as described in an embodiment at pages 207 to 212, amended independent claim 3 recites generating the routing tag as a sequence of quaternary symbols corresponding to one of three values, 0-bound, 1-bound, and bicast.

Lee does not teach or suggest either using a guide for routing a packet through a network nor does Lee disclose representing the output address of the network with quaternary symbols including a bicast state, (see below) as recited in amended claim 3. Lee at col. 8, lines 25-49 and Figs. 5 and 6 merely describes the architecture of the network and does not teach how a packet is routed through the network. Further, the Minimum Routing Number (MRN) generation logic described at col. 15, lines 53-58 is used to merely limit excessive bypassing during routing (col. 12, lines 11-48) and is not used for routing of a packet.

The Examiner appears to be stating that the switches used by Lee are somehow equivalent to sorting cells with the exception of the bicast value. As defined at page 159, lines

11-15 of the application, a sorting cell is a 2 x 2 switching element associated with a partially ordered input set, and the input signal switched to output-0 is never greater than the signal switched to output-1. A sorting cell which operates on the set{0, 1} where 0<1 has a truth table of:

Connection State		Input-1 control Signal	
		0	1
Input-0 Control Signal	0	Any	Bar
	1	Cross	Any

This operation is neither taught or suggested by Lee. The mere fact that two bits are used to control a switch setting is not determinative of the structure of the affected switch being a sorting cell, or for that matter any particular type of cell other than determining that the affected cell could have up to four switching states. Lee teaches a switch which bypasses a defeated packet from a routing contention where two or more packets are destined for the same output port (see col. 9, line 65 to col. 10, line 8) and does not teach or suggest a switch that has the characteristics of the sorting cell recited in amended claim 3.

Applicant submits that Yang et al. does not make up for the deficiencies of Lee. In the first instance, Yang et al. teaches a β element as the switching element in the network and does teach or suggest a sorting cell, as recited in amended claim 3. As described at col. 8, lines 46-56, a β element routes an input signal to an upper output if the control sequence bit is a "0" and routes the input signal to the lower output if the input signal is a "1". This is clearly not the logic employed by the claimed sorting cell (see above).

Also, the method disclosed by Yang et al. for constructing a routing tag is different from the claimed method. The method disclosed by Yang et al. requires a process that iterates over each control stage (col. 12, line 42 to col. 19, line 15) to determine the contents of the routing tag. In contrast, the amended claim 3, uses a characterization of the network referred to as a guide of the network, computed as the binary string $(\sigma_1\sigma_2 \ldots\sigma_{k-1})(n)$, $(\sigma_2 \ldots.\sigma_{k-1})(n)$, ..., $(\sigma_{k-2}\sigma_{k-1})(n)$, $\sigma_{k-1}(n)$, n. Such a string does not require computation by the iterative process taught by Yang et al.. Further, the method disclosed by Yang et al. is specific to a Benes type network. Advantageously, the method of amended claim 3 is applicable to any bit-permuting network, including but not limited to Banyan type networks, baseline networks, Omega networks and divide and conquer networks.

The Examiner further states that Yang et al. discloses at col. 10, lines 40-53, the idle and bicast values coded as 10 and 01. Such is not the case. As discussed above, the mere fact that a two bit code is used to control a switch is not determinative of the type of switching performed by the switch or the type of inputs switched by the switch.

Applicant submits that the combination of Lee and Yang et al. does not make amended claim 3 obvious. Accordingly Applicants respectfully request reconsideration and withdrawal of the §103 rejection of claim 3.

Further, it is respectfully submitted that since amended claim 3 has been shown to be allowable, claims 4-8 dependent on claim 3 are allowable, at least by their dependency. Accordingly, for all the above reasons, Applicants respectfully request reconsideration and withdrawal of the § 103 rejection of claims 4-8.

Claim 12

Claim 12 recites:

> A method for self-routing a plurality of real data packets *through a $2^n x 2^n$ switch, the switch having (a) 2^n external input ports, (b) 2^n external output ports labeled with 2^n distinct binary output addresses in the form of $b_1 b_2 .. . b_n$, (c) a plurality of switching cells interconnected into a k-stage bit-permuting network which is characterized by a guide $\gamma(1), \gamma(2), ..., \gamma(k)$ where γ is a mapping from the set {1, 2, ..., k} to the set {1, 2,..., n}, wherein each one of the switching cells is a sorting cell associated with the partial order "'0-bound' -< 'idle' < 'l-bound' and '0-bound' -< 'bicast'-< 'l-bound'", and (d) extra circuitry at the output end of each one of the switching cells, where the extra circuitry is composed of two parallel lxl switching elements, one at each one of the two output ports of the said each one of the switching cells, each one of the real data packets arriving at a distinct external input port determining an active input port and destined for a rectangular set of output addresses represented by a quaternary sequence $Q_1, Q_2, ..., Q_n$, where each Q_i is a quaternary symbol in any one of the*

three values: '0-bound', 'l-bound', and 'bicast', the method comprising:

generating an idle packet, which has no pre-determined destination output addresses, as a stream of '0' bits at each one of the non-active external input ports,

generating a routing tag $Q_{\gamma(1)}Q_{\gamma(2)}...Q_{\gamma(k)}$ for each one of the packets based on the guide of the bit-permuting network and the destination output addresses of the packet, wherein each $Q_{\gamma(j)}$ has one of the values of '0-bound', '1-bound', or 'bicast' for a real data packet, or has the value 'idle' for an idle packet,

routing each one of the packets through the network by using $Q_{\gamma(j)}$ in the routing tag of the packet in the j-th stage cell, $1 \leq j \leq k$, to select an output or both outputs from the j-th stage cell to emit the packet, and

processing the routing tag of each one of the packets by the extra circuitry at the output end of the j-th stage sorting cell before the said each one of the packets exiting from the said j-th stage cell by removing the leading quaternary symbol from the routing tag or rotating the leading quaternary symbol to the end of the routing tag such that the leading quaternary symbol of the routing tag of each one of the packets at each one of the j-th stage cells, $1 \leq j \leq k$, is always $Q_{\gamma(j)}$.

Applicant submits that claim 12 is non-obvious for essentially the same reasons that amended claim 3 is non-obvious, as discussed in detail above. In particular, neither Lee nor Yang et al. teach or suggest: (1) generating a routing tag based on a guide, (2) using sorting cells as switching elements or (3) representing output addresses as quaternary symbols having the values of 0-bound, 1-bound bicast or idle as recited in amended claim 12.

Applicant submits that the combination of Lee and Yang et al. does not make amended claim 12 obvious. Accordingly Applicants respectfully request reconsideration and withdrawal of the §103 rejection of claim 12.

Further, it is respectfully submitted that since amended claim 12 has been shown to be allowable, claims 13-16 dependent on claim 12 are allowable, at least by their dependency. Accordingly, for all the above reasons, Applicants respectfully request reconsideration and withdrawal of the § 103 rejection of claims 13-16.

Claim 17

Claim 17 recites:

A $2^n x 2^n$ self-routing switch comprising:

an array of 2^n external input ports and an array of 2^n external output ports with 2^n distinct binary output addresses in the form of $b_1 b_2 ... b_n$ for routing a packet, the packet being either a real data packet destined for a rectangular set of output addresses represented by a quaternary sequence $Q_1, Q_2, ..., Q_n$, where each Q_j is a quaternary symbol having one of the values of '0-bound', '1-bound' or 'bicast', or being an idle packet having no pre-determined destination output address,

a switching fabric having a plurality of switching cells interconnected into a k-stage bit-permuting network which is characterized by a guide $\gamma(1), \gamma(2), ..., \gamma(k)$, where γ is a mapping from the set $\{1, 2, ..., k\}$ to the set $\{1, 2, ..., n\}$,

routing tag circuitry, coupled to the external input ports, for generating a routing tag $Q_{\gamma(1)} Q_{\gamma(2)} ... Q_{\gamma(k)}$ for the packet based on the guide of the bit-permuting network and the destination addresses of the packet, and

routing control circuitry, coupled to the switching cells, for routing the packet through the switch by using $Q_{\gamma(j)}$ in the routing tag in the j-th stage cell, $1 \leq j \leq k$, to select an output or both outputs from

the j-th stage cell to emit the packet.

Applicant submits that claim 17 is non-obvious for essentially the same reasons that amended claims 3 and 12 are non-obvious, as discussed in detail above. In particular, neither Lee nor Yang et al. teach or suggest: (1) generating a routing tag based on a guide, or (2) representing output addresses as quaternary symbols having the values of 0-bound, 1-bound bicast or idle as recited in amended claim 17.

Applicant submits that the combination of Lee and Yang et al. does not make amended claim 17 obvious. Accordingly Applicants respectfully request reconsideration and withdrawal of the §103 rejection of claim 17.

Further, it is respectfully submitted that since amended claim 17 has been shown to be allowable, claims 18-21, dependent on claim 17 are allowable, at least by their dependency. Accordingly, for all the above reasons, Applicants respectfully request reconsideration and withdrawal of the § 103 rejection of claims 18-21.

Claims 9-11, 22-24 and 25.

Claims 9-11 and 25 are allowable based on their dependency on allowable claim 3. Claims 22-24 are allowable based on their dependency on allowable claim 17.

Conclusion

Insofar as the Examiner's objections and rejections have been fully addressed, the instant application, including claims 3-25, is in condition for allowance and Notice of Allowability of claims 3-25 is therefore earnestly solicited.

Respectfully submitted,

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August 3, 2005 By: _____
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